

1. Layer 1 Conformance Test

Test Suite: CHT-96-BA-L1 Verdicts Assigned
PASS: 06
FAIL: 0
INCONC:0

Selected Cases: 06

Test Identifier	ITU-T REC. I. 430	Verdict
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Test Group: Basic Interconnection Test

3.	Basic Interconnection Test	--(註)	PASS
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Test Group: Binary Organization of Frame

4.1.1	TEST A	5.4.2.1	PASS
4.1.2	TEST B	6.2.2	PASS

Test Group: Electrical Characteristics Test

6.8.2	Receiver Sensitivity	8.6.2.1	PASS
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Test Group: Power Feeding

7.1.1.1	NORMAL POWER PROVISION--TEST A	9.3.1.1	PASS
7.1.2.1	RESTRICTED POWER PROVISION--TEST A	9.3.2.1	PASS

註：'--' 表示無相對應章節。

2. Layer 2 Conformance Test

Test Suite: CHT-96-BA-L2

Verdicts Assigned

PASS:63

FAIL: 0

INCONC:0

Selected Cases: 63

Test Identifier

ITU-T REC. Q.921 Verdict

Test Group: DM70_V State 7.0 Valid Frms

DM70_V01	ID-Assigned : Ai Duplicated	5.3.2	PASS
DM70_V02	ID-Assigned : Ai Non Matching	5.3.2	PASS
DM70_V05	ID-Chk-Request : Ai Match	5.3.3.1	PASS
DM70_V06	ID-Chk-Request : Ai=127	5.3.3.1	PASS
DM70_V11	ID-Remove : Ai=127	5.3.4	PASS
DM70_V12	ID-Remove : Ai Match	5.3.4	PASS
DM70_V13	UA/F=1	5.8.7	PASS
DM70_V14	UA/F=0	5.8.7	PASS

Test Group: DM80_V State 8.0 Valid Frms

DM80_V01	ID-Assigned : Ai Duplicated	5.3.2	PASS
DM80_V02	ID-Assigned : Ai Non Matching	5.3.2	PASS
DM80_V05	ID-Chk-Request : Ai Match	5.3.3.1	PASS
DM80_V06	ID-Chk-Request : Ai=127	5.3.3.1	PASS
DM80_V11	ID-Remove : Ai=127	5.3.4	PASS
DM80_V12	ID-Remove : Ai Match	5.3.4	PASS
DM80_V13	UA/F=1	5.8.7	PASS
DM80_V14	UA/F=0	5.8.7	PASS

Test Group: DS70_V State 7.0 Valid Frms

DS70_V01	Window Rotation	5.9.5	PASS
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Test Group: DL70_V State 7.0 Valid Frms

DL70_V08	SABME/P=1	5.5.2	PASS
DL70_V10	SABME/P=0	5.5.2	PASS
DL70_V12	DISC/P=1	5.5.3.2	PASS
DL70_V13	DISC/P=0	5.5.3.2	PASS
DL70_V14	DM/F=0	5.7.1	PASS

DL70_V16	DM/F=1	5. 8. 7	PASS
DL70_V17	FRMR : Reject RR	5. 7. 1	PASS
DL70_V20	RR/P=1 : N(R)=V(S)	5. 6. 5	PASS
DL70_V21	RR/P=0 : N(R)=V(S)	5. 6. 5	PASS
DL70_V23	RR/F=0 : N(R)=V(S)	5. 6. 5	PASS
DL70_V30	REJ/P=1 : N(R)=V(S)	5. 6. 4	PASS
DL70_V31	REJ/P=0 : N(R)=V(S)	5. 6. 4	PASS
DL70_V32	REJ/F=0 : N(R)=V(S)	5. 8. 7	PASS
DL70_V36	RNR/P=1 : N(R)=V(S)	5. 6. 5	PASS
DL70_V37	RNR/P=0 : N(R)=V(S)	5. 6. 5	PASS
DL70_V39	RNR/F=0 : N(R)=V(S)	5. 6. 5	PASS
DL70_V44	I/P=1 : N(S)=V(R), N(R)=V(S)	5. 6. 2. 1	PASS
DL70_V45	I/P=0 : N(S)=V(R), N(R)=V(S)	5. 6. 2. 2	PASS
DL70_V46	I/P=1 : N(S)<>V(R), N(R)=V(S)	5. 8. 1	PASS
DL70_V47	I/P=0 : N(S)<>V(R), N(R)=V(S)	5. 8. 1	PASS
DL70_V57	T203 Timeout	5. 10. 3. 3	PASS
Test Group: DL80_V State 8.0 Valid Frms			
DL80_V08	SABME/P=1	5. 5. 2	PASS
DL80_V10	SABME/P=0	5. 5. 2	PASS
DL80_V12	DISC/P=1	5. 5. 3. 2	PASS
DL80_V13	DISC/P=0	5. 5. 3. 2	PASS
DL80_V14	DM/F=1	5. 7. 1	PASS
DL80_V15	DM/F=0	5. 7. 1	PASS
DL80_V17	FRMR : Reject RR	5. 7. 1	PASS
DL80_V20	RR/P=1 : V(A)<=N(R)<=V(S)	5. 6. 5	PASS
DL80_V21	RR/P=0 : V(A)<=N(R)<=V(S)	5. 6. 5	PASS
DL80_V22	RR/F=1 : V(A)<=N(R)<=V(S)	5. 6. 5	PASS
DL80_V23	RR/F=0 : V(A)<=N(R)<=V(S)	5. 6. 5	PASS
DL80_V24	REJ/P=1 : V(A)<=N(R)<=V(S)	5. 6. 4	PASS
DL80_V25	REJ/P=0 : V(A)<=N(R)<=V(S)	5. 6. 4	PASS
DL80_V26	REJ/F=1 : V(A)<=N(R)<=V(S)	5. 6. 4	PASS
DL80_V27	REJ/F=0 : V(A)<=N(R)<=V(S)	5. 6. 4	PASS
DL80_V28	RNR/P=1 : V(A)<=N(R)<=V(S)	5. 6. 5	PASS
DL80_V29	RNR/P=0 : V(A)<=N(R)<=V(S)	5. 6. 5	PASS
DL80_V30	RNR/F=1 : V(A)<=N(R)<=V(S)	5. 6. 5	PASS
DL80_V31	RNR/F=0 : V(A)<=N(R)<=V(S)	5. 6. 5	PASS
DL80_V32	I/P=1 : N(S)=V(R), N(R)=V(S)	5. 6. 2. 1	PASS
DL80_V33	I/P=0 : N(S)=V(R), N(R)=V(S)	5. 6. 2. 2	PASS

DL80_V34	I/P=1 : N(S)<>V(R), N(R)=V(S)	5. 8. 1	PASS
DL80_V35	I/P=0 : N(S)<>V(R), N(R)=V(S)	5. 8. 1	PASS
DL80_V44	T200 Timeout, RC=N200	5. 6. 7	PASS
DL80_V46	T200 Timeout, RC<N200, V(A)=V(S)	5. 6. 7	PASS

3. Layer 3 Conformance Test Summary Report

Test Suite: CHT-96-BA-L3	Verdicts Assigned
PASS: 57	
FAIL: 0	
INCONC: 0	

Selected Cases: 57

Test Identifier	ITU-T REC. Q.931	Verdict
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Test Group: Basic Interconnection Tests

1. Incoming Call (#21003)	5. 3. 3	PASS
2. Outgoing Call (#11105)	5. 3. 4	PASS
3. Outgoing Call (#11106) (A law call)	5. 3. 4	PASS
4. Outgoing Call (#11107) (U law call)	5. 3. 4	PASS

Test Group: U0 TESTS

#10001: [RC2(1,16), NO_MSG]	5. 8. 3	PASS
#10002: [RL3(1,16), RC_81]	5. 8. 3. 2b)	PASS
#10005: [SU3(BC, CD#, LLC, HLC), AL+CN+CP]	5. 2. 4	PASS
#10006: [SU2(SCI, BC, CD#, LLC, HLC), AL+CN+CP]	5. 2. 5	PASS
#10007: [SU6(BC, LLC, HLC), AL+CN+CP]	5. 2. 6	PASS
#10008: [SU4(IBCAP, LLC, HLC), RC_88+NO_MSG]	5. 2. 2	PASS
#20002: [<IUT!SETUP>, SU]	5. 1. 3	PASS

Test Group: U1 TESTS

#10101: [CP2, NO_MSG, U3]	5. 1. 5. 1	PASS
#10102: [RC2(1,16), NO_MSG, U0]	5. 8. 4	PASS
#10103: [RL3(1,16), RC]	5. 3. 2	PASS
#10106: [SQ2, ST]	5. 8. 10	PASS

Test Group: U3 TESTS

#10301: [AL2, NO_MSG, U4]	5. 1. 7	PASS
#10302: [CN2, ST(97,8,101)+SQ+CA+NO_MSG]	5. 1. 8	PASS

#10303:	[DI2(1,16), RL]	5.3.4	PASS
#10304:	[IN2(1), NO_MSG]	5.2.4	PASS
#10305:	[PG2, NO_MSG]	5.1.6	PASS
#10306:	[RC2(1,16), NO_MSG, U0]	5.8.4	PASS
#10307:	[RL3(1,16), RC]	5.3.4	PASS
#10308:	[SQ2, ST]	5.8.10	PASS
#20301:	[<IUT!DISC>, DI_16]	5.3.3	PASS
Test Group: U4 TESTS			
#10401:	[CN2, CA+NO_MSG]	5.1.8	PASS
#10402:	[DI2(1,16), RL]	5.3.4	PASS
#10403:	[IN2(1), NO_MSG]	5.2.4	PASS
#10404:	[PG2, NO_MSG ST]	5.1.6	PASS
#10405:	[RC2(1,16), NO_MSG, U0]	5.8.4	PASS
#10406:	[RL3(1,16), RC]	5.8.4	PASS
#10407:	[SQ2, ST]	5.8.10	PASS
#20401:	[<IUT!DISC>, DI_16]	5.3.3	PASS
Test Group: U8 TESTS			
#10801:	[CA2, NO_MSG, U10]	5.2.7	PASS
#10802:	[DI2(0,16), RL]	5.3.4	PASS
#10803:	[IN2(0), NO_MSG]	5.2.4	PASS
#10804:	[RC2(0,16), NO_MSG, U0]	5.8.4	PASS
#10805:	[RL3(0,16), RC]	5.3.2	PASS
#10806:	[SQ2, ST]	5.8.10	PASS
#20801:	[T313(4S) TIMEOUT, DI]	5.2.8	PASS
Test Group: U10 TESTS			
#11001:	[DI2(0,16), RL]	5.3.4	PASS
#11002:	[IN2(0), NO_MSG]	5.2.4	PASS
#11003:	[NO2(0), NO_MSG]	5.9	PASS
#11004:	[RC2(0,16), NO_MSG, U0]	5.8.4	PASS
#11005:	[RL3(0,16), RC]	5.8.4	PASS
#11006:	[SQ2, ST]	5.8.10	PASS
#21003:	[<IUT!DISC>, DI_16]	5.3.3	PASS
Test Group: U11 TESTS			
#11101:	[DI2(1,16), RL]	5.3.5	PASS
#11102:	[IN2(1), NO_MSG]	5.2.4	PASS
#11103:	[NO2(1), NO_MSG ST]	5.9	PASS
#11104:	[RC2(1,16), NO_MSG, U0]	5.8.4	PASS
#11105:	[RL3(1,16), RC]	5.3.4	PASS

#21101:	*[T305(30S) TIMEOUT, RL]	5.3.3	PASS
Test Group: U19 TESTS			
#11902:	[IN2(0), NO_MSG ST]	5	PASS
#11903:	[RC2(0,16), NO_MSG, U0]	5.3.4	PASS
#11904:	[RL3(0,16), NO_MSG, U0]	5.3.5	PASS
#11905:	[SQ2, ST]	5.8.10	PASS
#21901:	*[T308(4S) TIMEOUT, RL]	5.3.3	PASS